UNITRODE

UC1914
UC2914
UC3914

5V to 35V Hot Swap Power Manager

PRELIMINARY

FEATURES

- 5V to 35V Operation
- Precision Maximum Current Control
- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Overcurrent Limit
- Shutdown Control
- Charge Pump for Low RDS_{ON} High-Side Drive
- Latch Reset Function Available
- Output Drive V_{GS} Clamping
- Fault Output Indication
- 18 Pin DIL and SOIC Packages

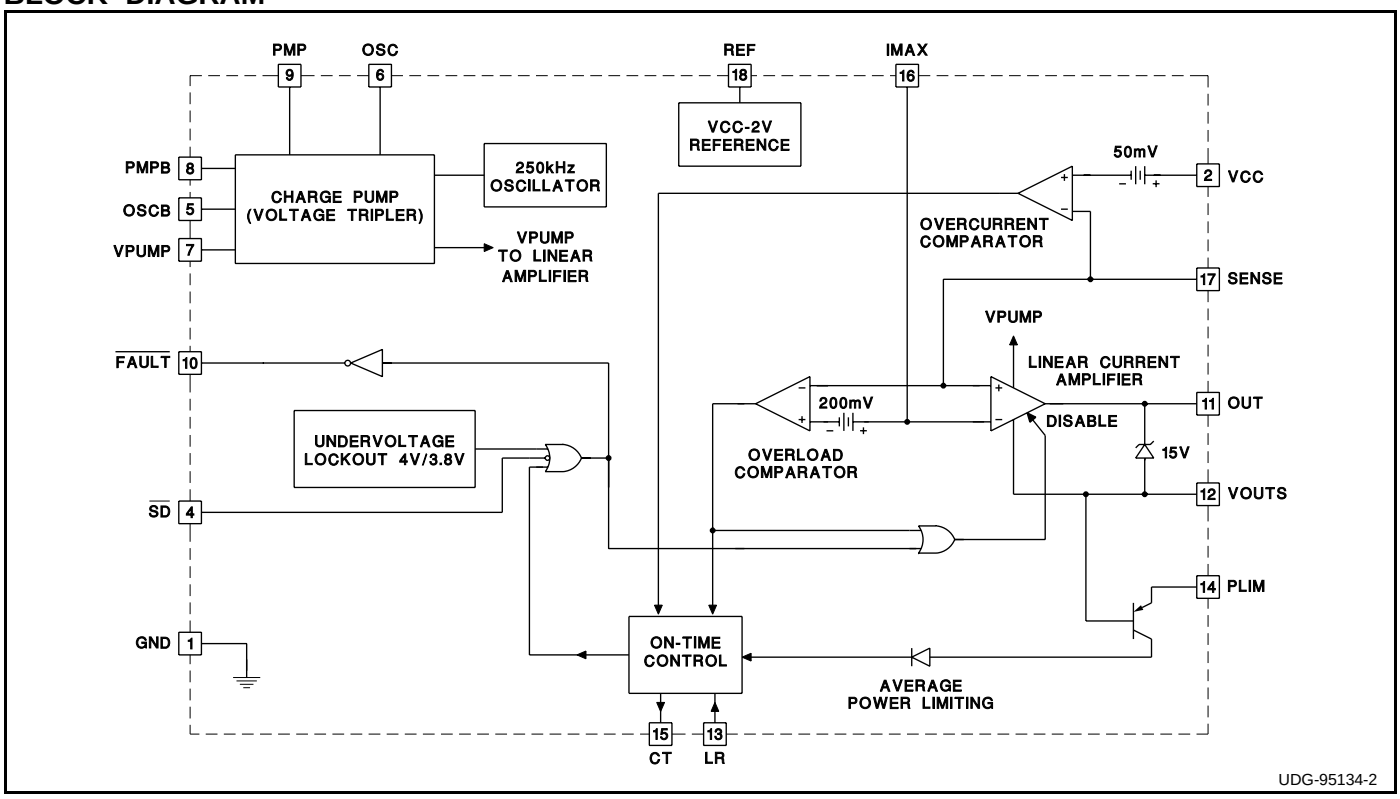
DESCRIPTION

The UC3914 family of Hot Swap Power Managers provides complete power management, hot swap and fault handling capability. Integrating this part and a few external components, allow a board to be swapped in or out upon failure or system modification without removing power to the hardware, while maintaining the integrity of the powered system. Complimentary output drivers and diodes have been integrated for use with external capacitors as a charge pump to ensure sufficient gate drive to the external NMOS transistor for low RDS_{ON}. All control and housekeeping functions are integrated and externally programmable and include the fault current level, maximum output sourcing current, maximum fault time and average power limiting of the external FET. The UC3914 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The fault level is fixed at 50mV with respect to VCC to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed by using a resistor divider from VCC to REF to set the voltage on IMAX. The maximum current level when the output appears as a current source is $(VCC - V_{IMAX})/R_{SENSE}$.

When the output current is less than the fault level, the external output transistor remains switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts to charge C_T, a timing capacitor. Once C_T charges to 2.5V, the output device is turned off and C_T is slowly discharged. Once C_T is discharged to 0.5V, the IC performs a retry and the output transistor is

(Continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

switched on again. The UC3914 offers two distinct reset modes. In one mode with LR left floating or held low, the IC will repeatedly try to reset itself if a fault occurs as described above. In the second mode with LR held high, once a fault occurs, the output is latched off until either LR is toggled low, the part is shutdown then re-enabled using $\overline{SD}$, or the power to the part is turned off and then on again.

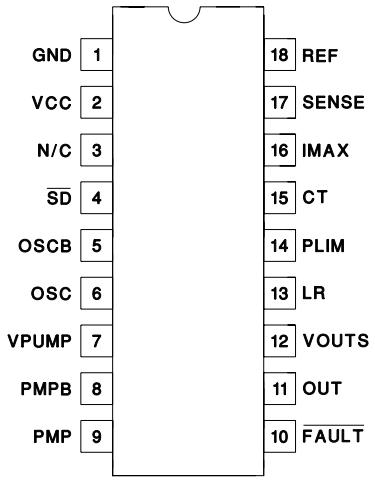
This part is offered in both 18 pin DW (SOIC) and Dual-In-Line (DIL) packages.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, VCC. 40V
Maximum Forced Voltage
  $\overline{SD}$ 12V
  IMAX VCC
  LR 12V
Maximum Current
  FAULT 20mA
  PLIM 10mA
Maximum Voltage, $\overline{FAULT}$ 40V
Reference Output Current . . . . . Internally Limited
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Unless otherwise indicated, voltage are reference to ground.
Currents are positive into, negative out of specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-18, SOIC-18 (Top View)
N or J Package, DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, VPUMP = VPUMP max, $\overline{SD}$ = 5V, CP1 = CP2 = C_{PUMP} = 0.01µF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Section					
I_{CC}			8	15	mA
	VCC = 35V		12	20	mA
Shutdown I_{CC}	$\overline{SD}$ = 0V		500	900	µA
UVLO	Turn on threshold		4	4.4	V
UVLO Hysteresis		100	200	350	mV
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C, Respect to VCC	–55	–50	–45	mV
	Over Operating Temperature, Respect to VCC	–57	–50	–42	mV
IMAX Input Bias			1	2.5	µA
CT Charge Current	CT = 1V	-125	–100	-75	µA
CT Discharge Current	CT = 1V	2	3	4.5	µA
CT Charge Current	CT = 1V, Overload Condition	–6	–3	–1.5	mA
CT Fault Threshold		2.25	2.5	2.75	V
CT Reset Threshold		0.45	0.5	0.55	V
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.5	3	4.5	%
Output Section					
OUT High Voltage	VOUTS = VCC, VPUMP = VPUMP max, with respect to VPUMP	–1.5	–1		V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, VPUMP = VPUMP max, $\overline{SD}$ = 5V, CP1 = CP2 = C_{PUMP} = 0.01µF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (cont.)					
OUT High Voltage	VOUTS = VCC, VPUMP = VPUMP max, IOUT = –2mA, with respect to VPUMP	–2	–1.5		V
OUT Low Voltage			0.8	1.3	V
	I_{OUT} = 5mA		1	2	V
	I_{OUT} = 25mA, Overload Condition, VOUTS = 0V		1.2	1.8	V
OUT Clamp Voltage	VOUTS = 0V	11.5	13	14.5	V
Rise Time	C_{OUT} = 1nF (Note 1)		750	1250	ns
Fall Time	C_{OUT} = 1nF (Note 1)		250	500	ns
Charge Pump Section					
OSC, OSCB Frequency		80	150	250	kHz
OSC, OSCB Output High	I_{OSC} = –5mA	10	11	11.6	V
OSC, OSCB Output Low	I_{OSC} = 5mA		0.2	0.5	V
OSC, OSCB Output Clamp Voltage	VCC = 25	18.5	20.5	22.5	V
OSC, OSCB Output Current Limit	High Side Only	–20	–10	–3	mA
Pump Diode Voltage Drop	I_{DIODE} = 10mA, Measured from PMP to PMPB, PMPB to VPUMP	0.5	0.9	1.3	V
PMP Clamp Voltage	VCC = 25	18.5	20.5	22.5	V
VPUMP Maximium Voltage	VCC = 12, VOUTS = VCC, Voltage Where Charge Pump Disabled	20	22	24	V
	VCC = 35V, VOUTS = VCC, Voltage Where Charge Pump Disable	42	45	48	V
VPUMP Hysteresis	VCC = 12, VOUTS = VCC, Voltage Where Charge Pump Reenabled	0.3	0.7	1.2	V
	VCC = 35V, VOUTS = VCC, Charge Pump Reenabled	0.3	0.7	1.2	V
Linear Current Section					
Input Offset Voltage		–15	0	15	mV
Voltage Gain		60	80		dB
IMAX Control Voltage	IMAX = OUT, SENSE = VCC, with Respect to VCC	–20	0	20	mV
	IMAX = OUT, SENSE = REF, with Respect to REF	–20	0	20	mV
SENSE Input Bias			1.5	3	µA
Reference Section					
REF Output Voltage	Respect to VCC	–2.25	–2	–1.75	V
REF Current Limit		12.5	20	50	mA
Load Regulation	I_{VREF} = 1mA to 10mA		25	60	mV
Line Regulation	VCC = 5V to 35V		25	100	mV
Shutdown Section					
Shutdown Threshold		0.6	1.5	2	V
Input Current	$\overline{SD}$ = 5V		150	300	µA
Delay to Output	(Note 1)		0.5	2	µs
Fault Section					
Fault Output Low	I_{FAULT} = 1mA		100	200	mV
Fault Output Leakage	V_{FAULT} = 35V		10	500	nA
Latch Section					
LR Threshold	High to Low	0.6	1.4	2	V
Input Current	LR = 5V		500	750	µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, VPUMP = VPUMP max, $\overline{SD}$ = 5V, CP1 = CP2 = CPUMP = 0.01µF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Limiting Section					
Duty Cycle Control	In Fault, I_{PLIM} = 200µA	0.6	1.3	2.0	%
	In Fault, I_{PLIM} = 3mA	0.05	0.12	0.2	%
Overload Section					
Delay to Output	(Note 1)		500	1250	ns
Threshold	Respect to IMAX	–250	–200	–150	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as:

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}}$$

where I_{CH} = 100µA + I_{PL}, and I_{PL} is the current into the power limit pin. Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = \frac{2 \bullet C_T}{I_{DIS}}$$

where Idis is nominally 3µA.

$\overline{FAULT}$: Open collector output which pulls low upon any of the following conditions: Timer fault, Shutdown, UVLO.

GND: Ground reference for the IC.

IMAX: This pin programs the maximum allowable sourcing current. Since REF is a –2V reference (with respect to VCC), a voltage divider can be derived from VCC to REF in order to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin, with respect to VCC, over the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on IMAX to VCC.

LR: If this pin is held high and a a fault occurs, the timer will be prevented from resetting the fault latch when CT is discharged below the reset comparator threshold. The part will not retry until this pin is brought to a logic low or a power-on-reset is caused. Pulling this pin low before the reset time is reached will not clear the fault until the reset time is reached. Floating or holding this pin low will result in the part repeatedly trying to reset itself if a fault occurs.

OUT: Output drive to the MOSFET pass element. Internal clamping ensures that the maximum V_{GS} drive is 15V.

OSC, OSCB: Complimentary output drivers for intermediate charge pump stages. A 0.01µF capacitor should be placed between OSC and PMP, and OSCB and PMPB.

PLIM: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to VCC. Current will flow into PLIM which adds to the fault timer charge current, reducing the duty cycle from the typical 3% level. When I_{PL} >> 100µA then the average MOSFET power dissipation is given by: P_{FET_AVG} = IMAX • 3 • 10^{-6} • R_{PL}.

PMP, PMPB: Complimentary pins which couple charge pump capacitors to internal diodes and are used to provide charge to the reservoir capacitor tied to VPUMP. Typical capacitor values used are 0.01µF.

REF: –2V reference with respect to VCC used to program the IMAX pin voltage. A 0.1µF ceramic or tantalum capacitor MUST be tied between this pin and VCC to ensure proper operation of the chip.

$\overline{SD}$: When this TTL compatible input is brought to a logic low, the output of the linear amplifier is driven low, $\overline{FAULT}$ is pulled low and the IC is put inot a low power mode.

SENSE: Input voltage from current sense resistor. When there is greater than 50mV across this pin with respect to VCC, a fault is sensed and C_T begins to charge.

VCC: Input voltage to the IC. Typical voltages are 4.5V to 35V. The minimum input voltage required for operation is 4.5V.

VOUTS: Source connection ot external N-channel MOSFET and sensed output voltage of load.

VPUMP: Charge pump output voltage. A capacitor should be tied between this pin and VOUTS with a typical value being 0.01µF.

APPLICATION INFORMATION

The UC3914 is to be used in conjunction with external passive components and an N-channel MOSFET (NMOS) to facilitate hot swap capability of application modules. A typical application set-up is given in Figure 7. The term hot swap refers to the system requirement that submodules be swapped in or out upon failure or system modification without removing power to the operating hardware. The integrity of the power bus must not be compromised due to the addition of an unpowered module. Significant power bus glitches can occur due to the substantial initial charging current of on-board module bypass capacitance and other load conditions (for more information on hot swapping and power management applications, see Application Note U-151). The UC3914 provides protection by monitoring and controlling the output current of an external NMOS to charge this capacitance and provide load current. The addition of the NMOS, a sense resistor, R_{SENSE}, and two other resistors, R1 and R2 set the programmed maximum current level the NMOS can source to charge the load in a controlled manner. The equation for this current, I_{MAX}, is:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}$$

where V_{IMAX} is the voltage generated at the IMAX pin. Analysis of the application circuit shows that V_{IMAX} (with respect to REF) can be defined as:

$$V_{IMAX} = \frac{(VCC - V_{REF}) \bullet R1}{R1 + R2} = \frac{2V \bullet R1}{R1 + R2}$$

where V_{REF} is the voltage is the voltage on the REF pin and whose internally generated potential is two volts below VCC. The UC3914 also has an internal overcurrent comparator which monitors the voltage between SENSE and VCC. If this voltage exceeds 50mV, the comparator determines that a fault has occurred, and a timing capacitor, C_T, will begin to charge. This can be rewritten as a current which causes a fault, I_{FAULT}:

$$I_{FAULT} = \frac{50mV}{R_{SENSE}}.$$

Fault Timing

Figure 1 shows the circuitry associated with the fault timing function of the UC3914. A typical fault mode, where the overload comparator and current source I3 do not factor into operation (switch S2 is open), will first be considered. Once the voltage across R_{SENSE} exceeds 50mV, a fault has occurred. This causes the timing capacitor, C_T, to charge with a combination of 100µA (I1) plus the current from the power limiting circuitry (I_{PL}).

Figure 2a shows typical fault timing waveforms for the external NMOS output current, the voltage on the CT pin, and the output load voltage, V_{OUT}, with LR left floating or grounded. The output voltage waveforms have assumed an RC characteristic load and time constants will vary depending upon the component values. Prior to time t_0, the load is fully charged to almost VCC and the NMOS is supplying the current, I_O, to the load. At t_0, the current begins to ramp up due to a change in the load conditions until, at t_1, the fault current level, I_{FAULT}, has been reached to cause switch S1 to close. This results in C_T being charged with the current sources I1 and I_{PL}. During this time, V_{OUT} is still almost equal to VCC except for small losses from voltage drops across the sense resistor and the NMOS. The output current reaches the programmed maximum level, I_{MAX}, at t_2. The C_T voltage continues to rise since I_{MAX} is still greater than I_{FAULT}. The load output voltage drops because the current load requirements have become greater than the controlled maximum sourcing current. The C_T voltage reaches the upper comparator threshold (Figure 1) of 2.5V at t_3, which promptly shuts off the gate drive to the NMOS (not shown but can be inferred from the fact that no output current is provided to the load), latches in the fault and opens switch S1 disconnecting the charging currents I1 and I_{PL} from C_T. Since no output current is supplied, the load voltage decays at a rate determined by the load characteristics and the capacitance. The 3µA current source, I2, discharges CT to the 0.5V reset comparator threshold. This time is significantly longer than the charging time and is the basis for the duty cycle current limiting technique. When the C_T voltage reaches 0.5V at t_4, the part performs a retry, allowing the NMOS to again source current to the load and cause V_{OUT} to rise. In this particular example, I_{MAX} is still sourced by the NMOS at each attempted retry and the fault timing sequence is repeated until time t_7 when the load requirements change to I_O. Since I_O is less than the fault current level at this time, switch S1 is opened, I2 discharges C_T and V_{OUT} rises to almost VCC.

Figure 2b shows fault timing waveforms similar to those depicted in Figure 2a except that the latch reset (LR) function is utilized. Operation is the same as described above until t_4 when the voltage on C_T reaches the reset threshold. Holding LR high prevents the latch from being reset, preventing the IC from performing a retry (sourcing current to the load). The UC3914 is latched off until either LR is pulled to a logic low, or the chip is forced into an under voltage lockout (UVLO) condition and back out of UVLO causing the latch to automatically perform a power on reset. Figure 2b illustrates LR being toggled low at t_5, causing the part to perform a retry. Time t_6 again illustrates what happens when a fault is detected. The LR pin is toggled low and back high at time t_7, prior to the volt-

APPLICATION INFORMATION (cont.)

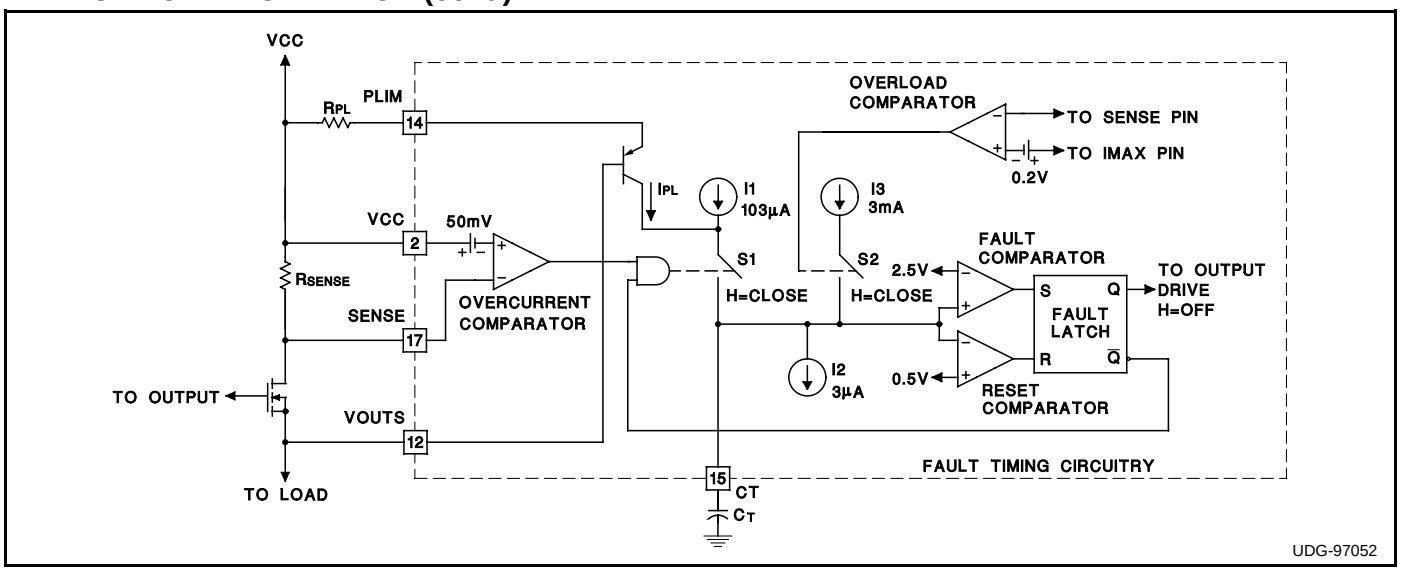


Figure 1. Fault Timing Circuitry for the UC3914, Including Power Limit and Overcurrent

age on the CT pin hitting the reset threshold. This information tells the UC3914 to allow the part to perform a retry when the lower reset threshold is reached, which occurs at t_8. Time t_9 corresponds to when load conditions change to where a fault is not present as described for Figure 2a.

Power Limiting

The power limiting circuitry is designed to only source current into the CT pin. To implement this feature, a resistor, R_{PL}, should be placed between VCC and PLIM. The current, I_{PL} (show in Figure 1) is given by the following expression:

$$I_{PL} = \frac{VCC - VOUTS}{R_{PL}}, \text{ for } VOUTS > 1V + VCT$$

where VCT is the voltage on the CT pin. For VOUTS < 1V + VCT the common mode range of the power limiting circuitry causes I_{PL} = 0 leaving only the 100µA current source to charge C_T. VCC - VOUTS represents the voltage across the NMOS pass device.

Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a fault condition where the output current is just above the fault level, but less than the maximum level, VOUTS ~ VCC, I_{PL} = 0 and the C_T charging current is 100µA.

During a fault, the CT pin will charge at a rate determined by the internal charging current and the external timing capacitor, C_T. Once C_T charges to 2.5V, the fault comparator trips and sets the fault latch. When this occurs, OUT is pulled down to VOUTS, causing the external NMOS to shut off and the charging switch, S1, to open. C_T will be discharged with I2 until the C_T potential reaches 0.5V. Once this occurs, the fault latch will reset (unless LR is being held high, whereby a fault can only be cleared by pulling this pin low or going through a power-on-reset cycle), which re-enables the output of the linear amplifier and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator will close the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{3\mu A}{I_{PL} + 100\mu A}$$

Average power dissipation can be limited using the PLIM pin. Average power dissipation in the pass element is given by:

$$P_{FET\,AVG} = (VCC - VOUTS) \bullet IMAX \bullet \text{Duty Cycle}$$

$$= (VCC - VOUTS) \bullet IMAX \bullet \frac{3\mu A}{I_{PL} + 100\mu A}$$

VCC – VOUTS is the drain to source voltage across the FET. When IPL >> 100µA, the duty cycle equation given above can be rewritten as:

$$\text{Duty Cycle} = \frac{R_{PL} + 3\mu A}{VCC - VOUTS}$$

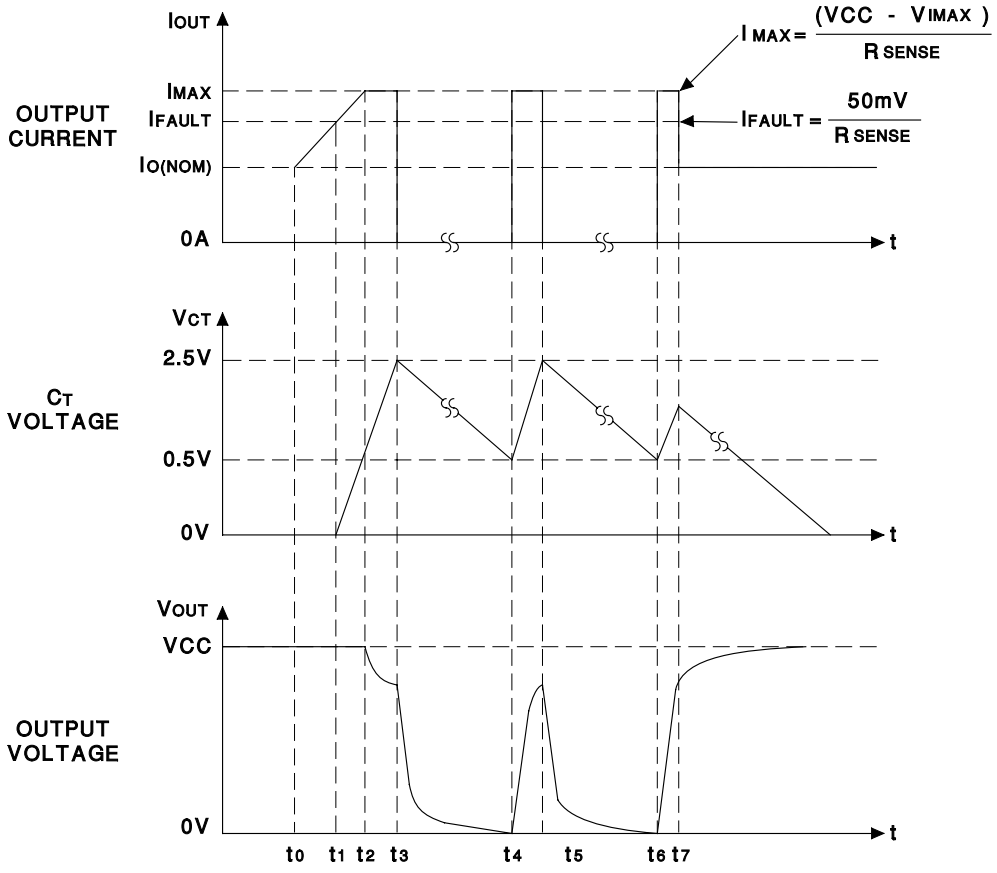
and the average power dissipation of the MOSFET is given by:

$$P_{FET\,AVG} = (VCC - VOUTS) \bullet IMAX \bullet \frac{R_{PL} + 3\mu A}{VCC - VOUTS}$$

$$= IMAX \bullet R_{PL} \bullet 3\mu A$$

The average power is limited by the programmed IMAX

APPLICATION INFORMATION (cont.)



t0: Normal conditions - output current is nominal, output voltage is at positive rail, VCC

t1: Fault control reached - output current rises above the programmed fault value, C_T begins to charge with ≅ 100µA + I_{PL}.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - C_T has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharge to GND.

t4: Retry - C_T has discharged to 0.5V, but fault current is still exceeded, C_T begins charging again, FET is on, VOUT increases.

t5 = t3: Illustrates <3% duty cycle depending upon R_{PL} selected.

t6 = t4

t7 = t0: Fault released, normal condition - return to normal operation of the hot swap power manager.

Figure 2a: Typical Timing Diagram

current and the appropriate value for R_{PL}.

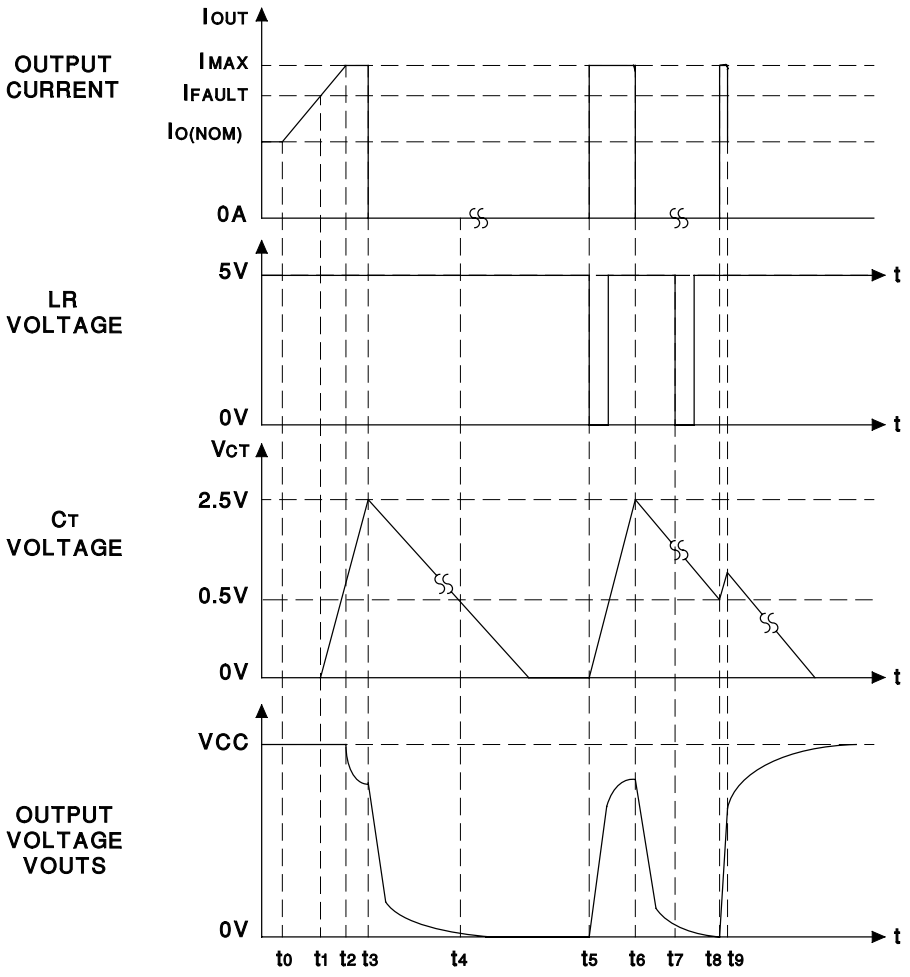
Overload Comparator

The linear amplifier in the UC3914 ensures that the external NMOS does not source more than the current I_{MAX}, defined above as:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}.$$

In the event that output current exceeds the programmed I_{MAX} by more than 200mV/R_{SENSE}, the output of the linear amplifier will immediately be pulled low (with respect to VOUTS) providing no gate drive to the NMOS, and preventing current from being delivered to the load. This situation could occur if the external NMOS is not responding to a command from the IC or output load conditions change quickly to cause an overload condition before the linear amplifier can respond. For example, if the NMOS is sourcing current into a load and the load suddenly becomes short circuited, an overload condition may occur. The short circuit will cause the V_{GS} of the NMOS to immediately increase, resulting in increased load current and voltage drop across R_{SENSE}. If this drop exceeds the overload comparator threshold, the amplifier

APPLICATION INFORMATION (cont.)



t0: Normal conditions - output current is nominal, output voltage is at positive rail, VCC

t1: Fault control reached - output current rises above the programmed fault value, C_T begins to charge with ≅ 100µA + I_{PL}.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - C_T has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharge to GND.

t4: Reset comparator threshold reached but no retry since LR pin held high.

t5 = t3: LR toggled low, NMOS turned on and sources current to load.

t6 = t3

t7: LR toggled low before V_{CT} reaches reset comparator threshold, causing retry.

t8: Since LR toggled low during present cycle, NMOS turned on and sources current to load.

t9 = t0: Fault released, normal condition - return to normal operation of the hot swap power manager.

Figure 2b. Typical Timing Diagram Utilizing LR (Latch Reset) Function

APPLICATION INFORMATION (cont.)

output will be quickly pulled low. It will also cause the CT pin to begin charging with I3, a 3mA current source (refer to Figure 1) and continue to charge until approximately one volt below VCC, where it is clamped. This allows a constant fault to show up on FAULT and since the voltage on CT will only charge past 2.5V in an overload fault condition, it can be used for detection of output NMOS failure or to build redundancy into the system.

Estimating Minimum Timing Capacitance

The startup time of the IC may not exceed the fault time for the application. Since the timing capacitor, C_T, determines the fault time, its minimum value can be determined by finding out the startup time of the IC. The startup time is dependent upon several external components. A load capacitor, C_{LOAD}, should be tied between VOUTS and GND. Its value should be greater than that of C_{PUMP}, the reservoir capacitor tied from VPUMP to VOUTS (see Figure 3). Given values of C_{LOAD}, Load, R_{SENSE}, VCC and the resistors determining the voltage on IMAX, the user can calculate the approximate startup time of the node VOUT. This time must be greater than the timer it takes for C_T to charge to 2.5V. Assuming the user has determined the fault current, R_{SENSE} can be calculated by:

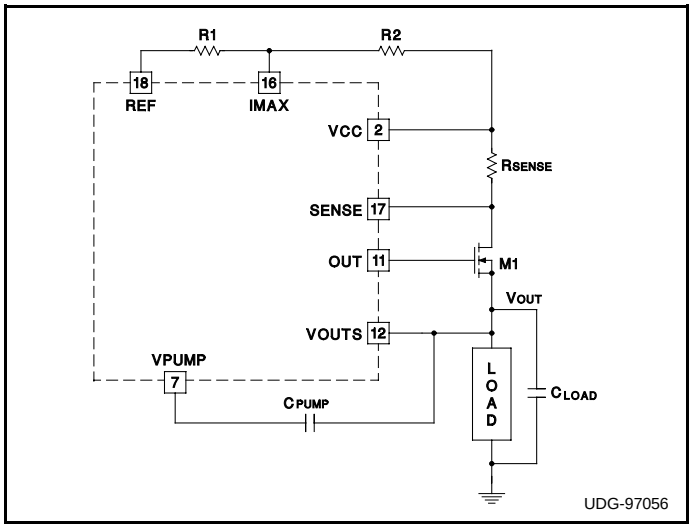


Figure 3. Estimating Minimum Timing Capacitor

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}.$$

I_{MAX} is the maximum current the UC3914 will allow through the transistor M1. During startup with an output capacitor, M1 can be modeled as a constant current source of value I_{MAX} where:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}$$

Given this information, calculation of startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{LOAD} \bullet VCC}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = R_{LOAD} \bullet C_{LOAD} \bullet \ln \bullet \left(1 - \frac{VCC}{I_{MAX} \bullet R_{LOAD}}\right)$$

The only remaining external component which may affect the minimum timing capacitor is the optional power limiting resistor, R_{PL}. If the addition of R_{PL} is desirable, its value can be determined from the "Fault Timing" section above. The minimum timing capacitor values are now given by

Current Source Load:

$$C_{T\ MIN} = 2 \bullet T_{START} \bullet \left(\frac{10^{-4} \bullet R_{PL} + \frac{VCC}{2}}{2 \bullet R_{PL}}\right)$$

Resistive Load:

$$C_{T\ MIN} = 2 \bullet \frac{(10^4 \bullet R_{PL} + VCC - I_{MAX} \bullet R_{LOAD}) \bullet T_{START}}{2 \bullet R_{PL}}$$

$$+ \frac{(I_{MAX} \bullet R_{LOAD}^2 \bullet C_{LOAD})}{2 \bullet R_{PL}}$$

Output Current Softstart

The external MOSFET output current can be increased at a user-defined rate to ensure that the output voltage comes up in a controlled fashion by adding capacitor, C_{SS}, as shown in Figure 4. The chip does place one constraint on the soft start time and that is that the charge pump time constant has to be much less than the soft-

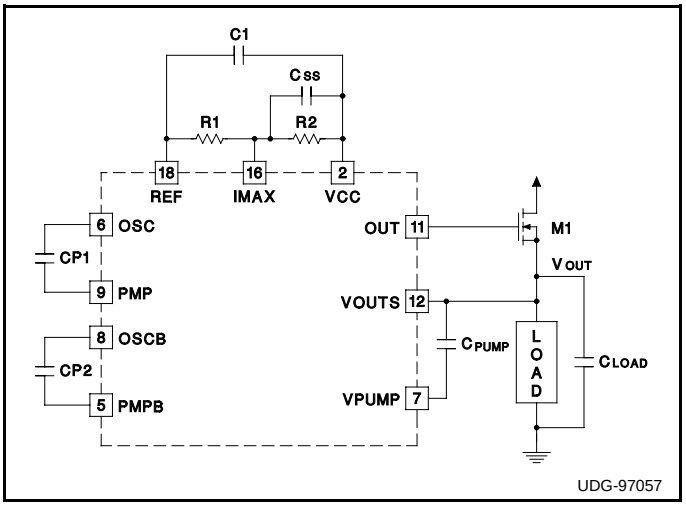


Figure 4. MOSFET Soft Start Diagram

APPLICATION INFORMATION (cont.)

start time constant to ensure proper soft start operation. The time constant determining the startup time of the charge pump is given by:

$$\tau_{CP} = R_{OUT} \bullet C_{PUMP}$$

ROUT is the output impedance of the charge pump given by:

$$R_{OUT} = \frac{1}{f_{PUMP} \bullet C_P}$$

where fPUMP is the charge pump frequency (125kHz) and CP = CP1 = CP2 are the charge pump flying capacitors. For typical values of CP1, CP2 and CPUMP (0.01µF) and a switching frequency of 125kHz, the output impedance is 800Ω and the charge pump time constant is 8µs. The charge pump should be close to being fully charged in 3 time constants or 24µs. By placing a capacitor from VCC to IMAX, the voltage at IMAX, which sets the maximum output current of the FET, will exponentially decay from VCC to the desired value set by R1 and R2. The output current of the MOSFET will be controlled via soft start as long as the soft start time constant (τ_{SS}) is much greater than the charge pump time constant τ_{CP}, given by

$$\tau_{SS} = (R1 \,||\, R2) \bullet C_{SS}$$

Minimizing Total Dropout under Low Voltage Operation

In a typical application, the UC3914 will be used to control the output current of an external NMOS during hot swapping situations. Once the load has been fully charged, the desired output voltage on the load, VOUT, will be required to be as close to VCC as possible to minimize total dropout. For a resistive load, RLOAD, the output voltage is given by:

$$V_{OUT} = \frac{R_{LOAD}}{R_{LOAD} + R_{SENSE} + RDS_{ON}} \bullet VCC$$

RSENSE was picked to set the fault current, IFAULT. RDSON, the on-resistance of the NMOS, should be made as small as possible to ensure VOUT is as close to VCC as possible. The equation to calculate RDSON is

$$RDS_{ON} = \frac{1}{\left(\mu C_{OX} \bullet \frac{W}{L_{EFF}} \bullet (V_{GS} - V_T)\right)}, \text{ for } V_{DS} < V_{GS} - V_T$$

where µ is the mobility of electrons in the channel, Cox is the per unit area capacitance of the gate, W is the width of the gate, LEFF is the effective channel length of the gate, VGS is the gate to source voltage, VDS is the drain to source voltage and VT is the threshold voltage of the device. For a given NMOS, the manufacturer will specify the RDSON for a certain VGS (maybe 7V to 10V). The source potential of the NMOS is VOUT. In order to ensure sufficient VGS, this requires the gate of the NMOS, which is the output of the linear amplifier, to be many volts above VCC. The UC3914 provides the capability to generate this voltage through the addition of 3 capacitors, CP1, CP2 and CPUMP as shown in Figure 5. These capacitors should be used in conjunction with the complimentary output drivers and internal diodes included on-chip to create a charge pump or voltage tripler. The circuit boosts VCC by charging capacitors CP1, CP2 and

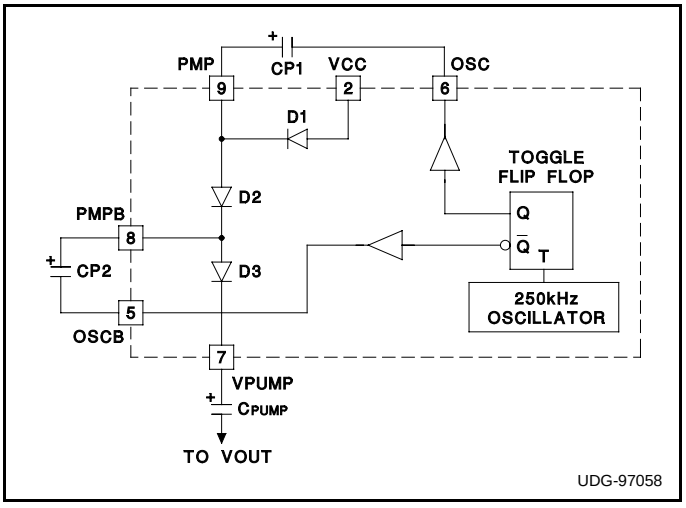


Figure 5. Charge Pump Block Diagram

CPUMP so that the voltage at VPUMP approximately equals 3 • (VCC - VDIODE), almost tripling the input supply voltage to the chip.

On each complete cycle, CP1 is charged up to approximately VCC – VDIODE (unless VCC is greater than 15V causing internal clamping to limit this charging voltage to about 13V) when the output Q of the toggle flip flop is low. When $\overline{Q}$ is transistioned low (and Q correspondingly is brought high), the negative side of CP2 is pulled to ground, and CP1 charges CP2 up to about 2 • VCC – 2 • VDIODE. When $\overline{Q}$ is toggled high, the negative side of CP2 is brought to VCC. Since the voltage across a capacitor cannot change instantaneously with time, the positive side of the capacitor swings up to 3 • VCC – 2 •VDIODE. This charges CPUMP up to 3 • VCC – 3 • VDIODE.

A circuit operating at the 4.5V minimum input supply voltage for the IC poses a potential issue in ensuring sufficient gate drive to the external NMOS. The desired output current sourcing limit of the external NMOS, IMAX, is set by:

$$\frac{VCC - V_{IMAX}}{R_{SENSE}}$$

but whether the MOSFET will actually be able to source

APPLICATION INFORMATION (cont.)

this current will depend upon what gate-to-source voltage is required to produce this current and other parameters discussed above. When the output device acts like a current source the drain current is given by:

$$I_D = \frac{\mu \bullet C_{OX}}{2} \bullet \frac{W}{L_{EFF}} \bullet (V_{GS} - V_T)^2, \text{ for } V_{DS} > V_{GS} - V_T$$

and is also equal to I_{MAX}, the programmed sourcing current. For a given FET, all device parameters in the above two equations are fixed including I_{MAX} and determine V_{GS}, provided enough charge pump voltage is available. When the NMOS acts like a resistor, the gate to source voltage wants to be maximized to ensure low RDS_{ON}. For a 4.5V input supply voltage, a maximum charge pump voltage of 11.4V is available, using the above equation for VPUMP = 3 • VCC - 3 • V_{DIODE}, and setting V_{DIODE} = 0.7V. This translates into only 6.9V of gate-to-source voltage when the voltage at the load, V_{OUT}, is pulled up to VCC. The maximum output voltage of the linear amplifier is actually less than this because of the ability of the amplifier to swing to within approximately 1V of VPUMP. Also, the charge pump drivers can only swing to within 100mV - 200mV of each rail and other inefficiencies in the charge transfer lead to even lower values of VPUMP and therefore V_{GS}. Operation under low input supply conditions may provide insufficient V_{GS} since typical threshold voltages for power MOSFETs range between 2V and 4V. Logic level MOSFETs can be used in place of standard power MOSFETs as they have lower threshold voltages (around 1V to 2V) but cannot provide nearly as much output current, which may exclude them for use in certain applications.

Figure 6 shows a way to use the existing drivers with external diodes (or schottky diodes for even higher pump voltages but with additional cost) and capacitors to make a voltage quadrupler. The additional charge pump stage will provide a sufficient pump voltage (VPUMP = 4 • VCC – 4 • V_{DIODE}) to generate the maximum V_{GS}. Operation is similar to the case described above. This additional circuitry is not necessary for higher input voltages because

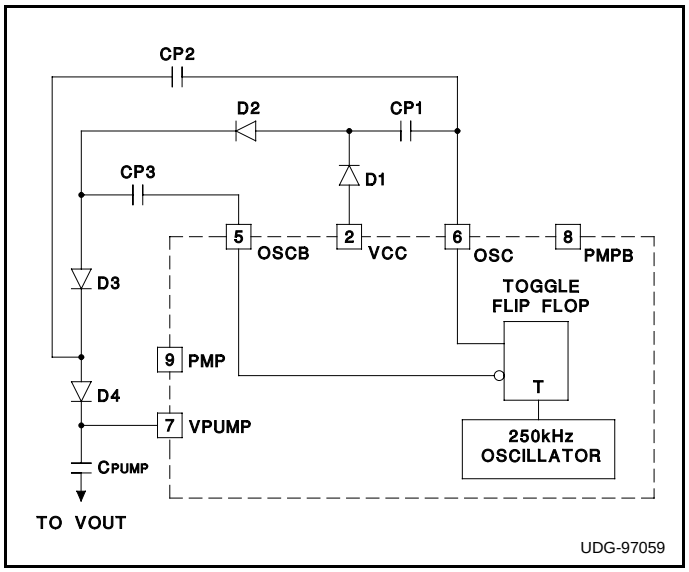


Figure 6. Low Voltage Operation to Produce Higher Pump Voltage

APPLICATION INFORMATION (cont.)

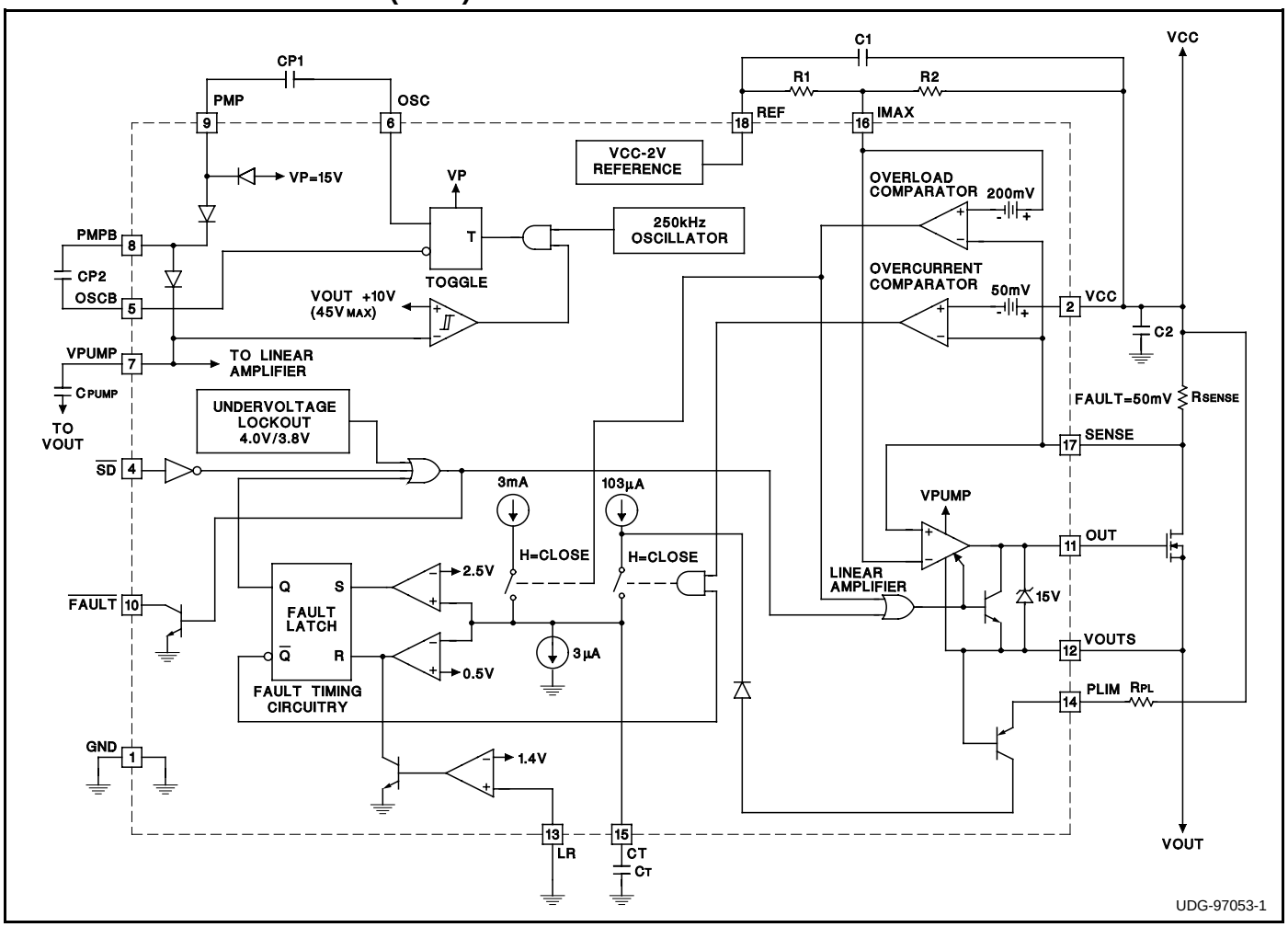


Figure 7. Typical Application

SAFETY RECOMMENDATIONS

Although the UC3914 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UC3914 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UC3914 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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